What is claimed is:

1. A method for erasing a nitride read only memory (NROM) block comprising a plurality of memory cells each having a gate input and two source/drain regions, the method comprising:
erasing the memory block; and
performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased.

2. The method of claim 1 wherein performing the recover operation includes coupling the gate input to a ramped voltage, a first source/drain region to a first constant voltage, and the remaining source/drain region to a second constant voltage.

3. The method of claim 1 wherein the ramped voltage starts in a range of -3 to 0V and ends in a range of 1 to 3V.

4. The method of claim 3 wherein the ramp voltage has a time period in a range of 10 microseconds to 1 second from start to end.

5. The method of claim 2 wherein the first constant voltage is in a range of 3 to 7V.

6. The method of claim 2 wherein the second constant voltage is in a range of 0 to 3V.

7. The method of claim 1 wherein the nitride read only memory cell is embedded in a CMOS device.

8. A method for erasing a nitride read only memory (NROM) block comprising a plurality of short-channel memory cells each having a gate input and two source/drain regions, the method comprising:

erasing the memory block; and

performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased, the recovery operation includes biasing each of the plurality of memory cells with a ramped voltage on the gate input, a constant voltage on a first source/drain region and the remaining source/drain region left floating.

9. The method of claim 8 and further comprising an oxide-nitride-oxide region, between the first and second source/drain regions, that can hold a single data bit.

10. The method of claim 8 wherein the constant voltage is in a range of 3 to 7V and the ramped voltage starts in a range of -3 to 0V and ends in a range of 1 to 3V over a time period in a range of 10 microseconds to 1 second.

11. The method of claim 8 wherein erasing the memory block includes biasing each of the plurality of cells with a first constant voltage on the gate input, a second constant voltage on a first source/drain region, and a third constant voltage on the remaining source/drain region.

12. The method of claim 11 wherein the first constant voltage is in a range of –12 to 0, the second constant voltage is in a range of 3 to 8V, and the third constant voltage is in a range of 3 to 8V.

13. The method of claim 11 wherein the first source/drain region acts as a drain connection and the remaining source/drain region acts as a source region.

14. The method of claim 13 wherein the source region is allowed to float.

15. A method for erasing a nitride read only memory (NROM) block comprising a plurality of short-channel memory cells each having a gate input and two source/drain regions, the method comprising:

erasing the memory block;

verifying erasure of the memory block; and

if erasure is not complete, performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased.

16. The method of claim 15 wherein verifying comprises performing a read operation and checking for column current such that a presence of column current indicates that erasure is not complete.

17. A nitride read only memory device comprising:

a plurality of memory cells, each memory cell comprising:

a gate input that is biased with a constant voltage during an erase operation and a ramped voltage during a subsequent recovery operation to raise its threshold voltage;

a first source/drain region acting as a drain connection that is biased with a constant voltage during both the erase operation and the subsequent recovery operation; and

a second source/drain region acting as a source connection that is either coupled to a constant voltage or allowed to float during both the erase operation and the subsequent recovery operation.

18. The device of claim 17 wherein the plurality of memory cells is embedded in a CMOS device.

19. The device of claim 17 and further including a channel between the first and second source/drain regions that is less than 2 microns in length.

20. An electronic system comprising:

a processor that generates control signals; and

a nitride read only memory, coupled to the processor, for storing data in response to the control signals, the memory comprising:

a plurality of memory cells, each memory cell comprising:

a gate input that is biased with a constant voltage during an erase operation and a ramped voltage during a subsequent recovery operation to raise its threshold voltage;

a first source/drain region acting as a drain connection that is coupled to a constant voltage during both the erase operation and the subsequent recovery operation; and

a second source/drain region acting as a source connection that is either coupled to a constant voltage or allowed to float during both the erase operation and subsequent recovery operation.

21. The electronic system of claim 19 wherein the processor and nitride read only memory are embedded together in one integrated circuit.